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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

DUONG, THOI V

ART UNIT

PAPER NUMBER

2871

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/750,342

Applicant(s)

PARK ET AL.

Examiner

Thoi V Duong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6 and 9 is/are allowed.
- 6) ☒ Claim(s) 1-4 and 14 is/are rejected.
- 7) ☒ Claim(s) 5,7,8 and 10-13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

1. This office action is in response to the Amendment, Paper No. 6, filed January 16, 2003.

Accordingly, claims 1, 6, 9 and 14 were amended. Currently, claims 1-14 are pending in this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Shiba et al. (USPN 5,684,555).

As shown in Figs. 1-4, Shiba discloses a liquid crystal display device comprising:
upper and lower substrates 500 and 200 with a liquid crystal layer 600 interposed therebetween;

a sealant 113 between the upper and lower substrates in an area near an edge of the upper substrate 500;

a plurality of source pads 761-764 (Fig. 3) and gate pads (not shown) on the lower substrate 200;

a plurality of gate lines Yij and data lines Xi on the lower substrate (col. 3, line 56 through col. 4, line 8), each gate line being electrically connected with the

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corresponding gate pad, each data line being electrically connected with the corresponding source pad (col. 4, lines 57-65);

a gate insulating layer 211 between the gate lines and the data lines;

a source PCB 800 and a gate PCB 900 electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area 111 in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB (Fig. 1);

a plurality of transmitting wires 123-1 to 123-4 on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant (col. 5 line 67 through col. 6, line 5) such that the source PCB is electrically connected with the gate PCB through a counter electrode 541 (col. 6, lines 43-46); and

a plurality of switching devices 221,

wherein each transmitting wire has 5 narrow lines which are guided across the sealing area 111 (col. 6, lines 7-16).

Finally, Shiba discloses that, depending on the kind of the TFTs, the transmitting wires can be formed in the same step of forming the gate lines (col. 6, lines 33-35).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiba et al. (USPN 5,684,555) in view of Kuwashiro (USPN 5,945,984).

Shiba discloses a LCD device that is basically the same as that recited in claim 4 except for a plurality of dummy pads between the adjacent gate pads and between the adjacent source pads. As shown in Fig. 3, Kuwashiro discloses a LCD device in which dummy pads 731-1, 731-2 are disposed between data pads 721 for inspecting and repairing the display. Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD device of Zhang with the teaching of Kuwashiro by forming a plurality of dummy pads between the adjacent gate pads and between the adjacent source pads so as to easily perform an inspection and repair the display.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (USPN 5,995,189) in view of Noritake et al. (USPN 6,400,438 B1).

As shown in Figs. 1-6, Zhang discloses a method of fabricating a liquid crystal display device, the method comprising:

- preparing first and second substrates;

- forming a plurality of gate lines 106, gate pads, gate transmitting lines 109 and dummy patterns 301 on the first substrate 201 (col. 6, lines 63-67, col. 7, lines 1-6, and col. 10, line 64 through col. 11, line 4);

- forming a gate insulating layer 220 on the gate lines, gate pads, gate transmitting wires, and dummy patterns;

- forming a plurality of data lines 105 and data pads, on the gate insulating layer;

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forming a passivation layer 227 on the data lines and the data pads;
forming a sealant 107 on the first substrate (col. 11, lines 49-59);
attaching the first and second substrates and forming a liquid crystal layer
between the first and second substrates (col. 11, lines 60-67).

Zhang discloses a method of fabricating a liquid crystal display device that is basically the same as that recited in claim 14 except for scribing and breaking the second substrate. Referring to Fig. 5(a), Noritake discloses that insulator substrates 12a-12d are cut away by means of scribing and breaking a mother glass board 31 along the dotted line in Fig. 5(a) wherein the edges of the contact portions 22 of an opposite electrode 17 (Fig. 6) do not extend beyond or to the borders of the substrates 12a-12d and each separated substrate 12 is used to fabricate a LCD as shown in Fig. 6 (col. 3, lines 62-67 and col. 4, lines 1-8). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of fabricating a LCD device of Zhang with the teaching of Noritake by scribing and breaking the second substrate so as to create separated liquid crystal panels without contaminants and hence improve reliability of the display.

Allowable Subject Matter

7. Claims 5, 7, 8, 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

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In addition to other elements as shown in claim 1, none of the prior art of record suggests or discloses alone or in combination that a liquid crystal display device further comprises:

a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire;

or

first and second repair wires, the first repair wire crossing with each of the source pads with the gate insulating layer interposed therebetween, the second repair wire crossing with each of the gate pads with the gate insulating layer interposed therebetween;

or

first and second dummy patterns on the lower substrate, the first dummy pattern being positioned along a first edge of the upper substrate, the second dummy pattern being positioned along a second edge of the upper substrate, the each dummy pattern having at least the same height as the gate transmitting wire.

The most revelant references, USPN 5,684,555 of Shiba et al. and USPN 5,995,189 of Zhang, fail to disclose or suggest a liquid crystal display comprising a source PCB and a gate PCB electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB; a plurality of transmitting wires being electrically connected with the gate and source pads across the sealant such that the

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source PCB is electrical connected with the gate PCB; a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire; and first and second dummy patterns on the lower substrate, wherein each dummy pattern has at least the same height as the gate transmitting wire. The Shiba's reference only discloses a liquid crystal display device comprising a source PCB and a gate PCB electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB, and a plurality of transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrical connected with the gate PCB. Meanwhile, the Zhang's reference discloses a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire, and first and second dummy patterns on the lower substrate, wherein each dummy pattern has at least the same height as the gate transmitting wire; however, the source PCB and the gate PCB are formed inside the area in which the sealant is formed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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8. Claims 6 and 9 are allowed for the same reasons set forth in the last office action for claims 6, 9 and 11.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

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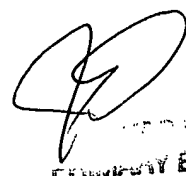
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong

04/02/2003


THOI DUONG
PATENT EXAMINER